

Ivan Papusha

CONTACT INFORMATION	Ivan Papusha 1200 E. California Blvd. MC 305-16 Pasadena, CA 91125	ipapusha@caltech.edu www.ivanpapusha.com (703) 399-5010 Updated: February 6, 2012
EDUCATION	California Institute of Technology , Pasadena, CA <ul style="list-style-type: none">Ph.D. Control and Dynamical Systems, $Et_{grad} = 2015$ Stanford University , Stanford, CA <ul style="list-style-type: none">M.S. Electrical Engineering, 2011 <i>Specialization: Dynamic Systems and Optimization.</i>B.S. Electrical Engineering, Physics minor, 2011 <i>Specialization: Circuits and Devices.</i> Thomas Jefferson High School for Science and Technology , Alexandria, VA <ul style="list-style-type: none">Advanced Studies Diploma, 2007	
WORK/RESEARCH EXPERIENCE	Research Analyst Intern , AOL Advertising.com, Palo Alto, CA Performed ad placement valuation for AdLearn with the Prediction and Bidding R&D team.	2011
	CURIS Researcher , Stanford Artificial Intelligence lab, Stanford, CA Developed algorithms to train Deep Belief Networks (DBNs) for image classification.	2010
	REU Researcher , Stanford Center for Integrated Systems, Stanford, CA Built circuitry to enable lithography with a Scanning Electron Microscope (SEM).	2009
	Engineering Intern , Naval Research Laboratory, Washington, DC Analyzed hyperspectral data on a Cray XD1 supercomputer.	2006-2008
TEACHING EXPERIENCE	Teaching Assistant , Stanford University <ul style="list-style-type: none">EE 263: Linear Dynamical Systems (grad)EE 364a: Convex Optimization I (grad)EE 102b: Signal Processing and Linear Systems II (undergrad) Appointment/Resident Tutor , Stanford CTL, Stanford, CA Tutored students one-on-one in math, physics, and engineering.	2010-2011 2009-2011
TECHNICAL SKILLS	Programming: C++, Python, Java, and other languages (that matter) Analysis and simulation: Matlab, Mathematica, CVX Hardware and systems: Verilog, Cadence, SPICE, AVR microcontrollers, PCB layout Parallel computing: OpenMP, MPI, Hadoop Languages: Russian (fluent), German (conversational) Interests: I am a scholar and tinkerer; therefore, I like to tinker with things and be scholarly.	
HONORS AND AWARDS	Division Fellowship, Caltech CDS Department, 2011 Business Association of Stanford Entrepreneurial Students (BASES) Forge project grant, 2011 Armed Forces Communications and Electronics Association (AFCEA) scholarship, 2008-2010 Microchip PIC design contest Phase 1, 2008 Naval Research Lab, SEAP Symposium Award, 2006 SIAM, student member	
KEYWORDS	control theory, convex optimization, machine learning, signal processing, robotics, systems engineering, embedded devices, FPGAs, financial applications, cloud computing.	